IN THE CLAIMS

1. **(Currently Amended)** [[An]] A system including an electronic device containing protected data, the electronic device comprising:

a local processor;

memory protection logic operable to interface with memory for ~~storing~~ accessing protected data stored therein, wherein access to said protected data is restricted for access by [[a]] said local processor for execution thereon within said device;

validation logic, operative in a first mode, for checking the validity of said protected data and for producing a validity signal to determine whether said protected data is valid, said validation logic being accessible from the outside of the electronic device for setting the electronic device into said first mode; ~~and~~

validity signal output control logic for inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked;

a system reset function for resetting the system including at least said local processor; and

a device reset function for resetting said validation logic in response to said system being reset while the electronic device is in said first mode.

2. **(Currently Amended)** The ~~device~~ system of claim 1, wherein said validity signal output control logic inhibits the output of said validity signal until the validity of all said protected data has been checked.

3. **(Currently Amended)** The ~~device~~ system of claim 1, further comprising means operative in said first mode for transferring said data to be checked to said validation logic by cycling through successive memory addresses.

4. **(Currently Amended)** The ~~device~~ system of claim 1, wherein said validation logic performs an algorithm involving each item of said protected data to be checked and yielding said validity signal in the form of a value resulting from said algorithm.

5. **(Currently Amended)** The ~~device~~ system of claim 4, wherein said algorithm IS a checksum calculation.

6. **(Currently Amended)** The ~~device~~ system according to claim 1, wherein said protected data is bound by first and second extremity addresses, said device comprising mode control means authorizing access into said first mode only when said first extremity address of said memory is selected as a starting point for transferring data therefrom to said validation logic.

7. **(Currently Amended)** The ~~device~~ system according to claim 6, wherein said mode control means causes an exit from said first mode after said second extremity address has been attained.

8. **(Currently Amended)** The ~~device~~ system according to claim 1, wherein said validity signal output control logic is operative to inhibit said output of said validity signal all the while said first mode is active.

9. **(Currently Amended)** The ~~device~~ system of claim 1, provided with a device reset function, wherein said device further comprises reset means for resetting said validation logic in response to a device reset in said first mode.

10. **(Currently Amended)** The ~~device~~ system of claim 1, provided with a device reset function, wherein said device further comprises means for exiting from said first mode upon a device reset.

11. **(Currently Amended)** The ~~device~~ system of claim 10, wherein said device reset function comprises latching means for temporarily latching a logic state indicating the presence of the first mode and gating means for transferring the device reset signal to a reset input of the validation logic only when said logic state is present in the latching means, the latching means temporarily maintaining said gating means enabled after a disappearance of the logic state caused by the device reset signal.

12. **(Currently Amended)** The ~~device~~ system of claim 1, further comprising reset means operative to reset said validity signal upon said device being forced to leave said first mode prematurely.

13. **(Currently Amended)** The ~~device~~ system of claim 1, wherein said validity signal output control logic comprises gating means for controllably transferring said validity signal to outside said device, said gating means having an inhibit input connected to receive a mode signal for inhibiting transfer of said validity signal all the while said first mode is active.

14. **(Currently Amended)** The ~~device~~ system of claim 1, wherein said memory means comprises a chip select or chip enable input, said input being connected to selection means for delivering an enable signal when a first mode selection signal[[,]] and a protection Option signal are active.

15. **(Currently Amended)** The ~~device~~ system of claim 14, wherein said selection means delivers said enable signal on a further condition that an address belonging to said memory means has been selected at an address input thereof.

16. **(Currently Amended)** The ~~device~~ system of claim 1, wherein at least said memory and said checking device are formed on a common chip and interconnected by an internal bus.

17. **(Currently Amended)** The ~~device~~ system of claim 1, wherein said memory means is a read-only memory.

18. **(Currently Amended)** The ~~device~~ system of claim 1, wherein said protected data comprises program code.

19. **(Currently Amended)** The ~~device~~ system of claim 1, implemented in a microcontroller unit or microprocessor chip.

20. **(Currently Amended)** A method of protecting data contained in memory of an electronic device of a system, the method comprising:

coupling memory protection logic to interface with memory for ~~storing~~ accessing protected data stored therein, wherein access to said protected data is restricted for access by [[a]] said local processor for execution thereon within said device;

from outside of the electronic device, checking[[, during a first mode,]] the validity of said protected data [[and]], producing a validity signal indicative of whether said protected data is valid, and setting the electronic device into a first mode;

inhibiting an output of said validity signal to outside said device until the validity of a predetermined quantity of said protected data has been checked;

resetting the system including at least said local processor; and

resetting said validation signal in response to resetting the system while the electronic device is in said first mode.

21. **(Previously Presented)** The method of claim 20, wherein said validity signal output control means inhibits the output of said validity signal until the validity of all said data to be protected has been checked.

22. **(Previously Presented)** The method of claim 20, wherein said data to be checked is checked by cycling through successive memory addresses.

23. **(Original)** The method of claim 20, wherein said check involves performing an algorithm on each item of said protected data to be checked and yielding said validity signal in the form of a value resulting from said algorithm.

24. **(Original)** The method of claim 23, wherein said algorithm is a checksum calculation.

25. **(Previously Presented)** The method of claim 20, wherein said protected data is bound by first and second extremity addresses, and access into said first mode is authorized only when said first extremity address of said memory is selected as a starting point for transferring data therefrom to said checking.

26. **(Previously Presented)** The method according to claim 25, wherein said access into said first mode is authorized only when said first extremity address along with said second extremity address has been selected.

27. **(Original)** The method according to claim 20, wherein said output of validity signal is inhibited all the while said first mode is active.

28. **(Previously Presented)** The method of claim 20, further comprising the step of resetting a validity signal in response to a device reset in said first mode.

29. **(Original)** The method of claim 20, further comprising the step of exiting from said first mode upon a device reset.

30. **(Previously Presented)** The method of claim 29, further comprising the step of temporarily latching a logic state indicative of the presence of said first mode and controllably passing said device reset signal to a reset input of said checking when said logic state is latched.

31. **(Original)** The method of claim 20, further comprising the step of resetting said validity signal upon said device being forced to leave said first mode prematurely.

32. **(Previously Presented)** The method of claim 20, further comprising the step of controllably inhibiting the transfer of said validity signal to outside said device when said first mode is active.

33. **(Previously Presented)** The method of claim 20, further comprising the step of delivering to a chip select or chip enable input of said memory means an enable signal when a first mode selection signal, and a protection option signal are active.

34. **(Original)** The method of claim 33, further comprising the step of delivering said enable signal on the further condition that an address belonging to said memory means has been selected at an address input thereof.

35. **(Original)** The method of claim 20, wherein said protected data comprises program code.

36. **(Previously Presented)** The method of claim 20, implemented in a microcontroller unit or microprocessor chip.